Amendments to the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 10/074,453, filed February 11, 2002. --

Please amend the paragraph beginning at page 12, line 14 as follows:

At this point during the first discharge mode, the voltages VPP on the array source AS and p-well drive PWDRV discharge through the diode-coupled transistors 354, 360 and the voltage on the array source and p-well drive begins decreasing as illustrated. Note the voltage –VPP on the word line WL also begins increasing towards ground at this time. The discharge of the word line WL directly to ground slightly affects the discharge of the array source AS and p-well drive PWDRV, as indicated by the level portion 370 ~~500~~ of the discharge voltage curves for the array source and p-well drive between the time T0 and a time T1. No increase in the voltages on the array source AS and p-well drive PWDRV results from this coupling of the word line discharge. Moreover, also note the discharge of the array source AS and p-well drive PWDRV does not affect the voltage on the word line WL as in the prior art.

Please amend the paragraph beginning at page 12, line 25 as follows:

The discharge controller 300 discharges the voltages on the array source AS, p-well drive PWDRV, and word line WL to ground as illustrated in Figure 5A after the time T0. The controller 300 operates in the first discharge mode from the time T0 until at time T2, at which point the DIS2 signal goes high to initiate the second discharge mode of operation. The DIS1 signal remains high during the second discharge mode, causing the first level-shifting circuit 302 to maintain the HVDIS1 signal high. In response to the high DIS2 signal, the second level shifting circuit 316 drives the HVDIS2 signal high as shown in Figure 5B after the time T2. When the HVDIS2 signal goes high, the bypass transistors 356, 362 (Figure 4) turn ON,

bypassing the diode-coupled transistors 354, 360 and discharging the array source AS and p-well drive PWDRV to ground through the transistors 352, 356 and 358, 362. The voltages on the array source AS and p-well drive PWDRV begin discharging to ground, as illustrated by the portion 372 ~~500~~ of these voltage curves at just after the time T2.